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SUPERSEDING
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MILITARY SPECIFICATION

# MICROCIRCUIT, DIGITAL, 32,768 BIT MOS, ULTRAVIOLET ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EPROM) MONOLITHIC SILICON

This specification is approved for use by the Department of the Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

## 1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic, silicon, N-channel MOS erasable programmable read-only memory microcircuits which employ the ultraviolet light erasing technique. One product assurance classes and a choice of case outline/lead material and finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510. The "JAN" or "J" certification mark shall not be used.

1.2.1 Device type. The device type shall be as follows:

| Device type | Circuit |
|---|---|
| 01 | 4096 X 8 bit EPROM |

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outline shall be designated as follows:

| Letter | Case outline (see MIL-M-38510/, appendix C) |
|---|---|
| J | D-3 (24-lead, 1/2" X 1-1/4") dual-in-line package 1/ |

1.3 Absolute maximum ratings.

| | |
|---|---|
| Supply voltage, $V_{CC}$ 2/ | -0.3 to 6.0 V |
| All input or output voltages 2/ | -0.3 to 6.0 V |
| Program input, $V_{pp}$ | -0.3 to 28.0 V |
| Operating case temperature range | -55° to +125°C |
| Storage temperature range | -65° to +125°C |
| Lead temperature (soldering, 10 sec) | 300°C |
| Thermal resistance, junction-to-case | $\theta_{JC}$ = 30°C/W |
| Maximum power dissipation, $P_D$ | 1.0 Watts DC<br>1.8 Watts DC during programming |
| Junction temperature ($T_J$) | +160°C |

1/ The lid shall be transparent to permit ultraviolet light erasure.

2/ Under absolute maximum ratings, voltage values are with respect to ground, unless otherwise specified. Throughout the remainder of this data sheet, voltage values are with respect to ground.

Beneficial comments (recommenations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBE-2, Griffis AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage, $V_{CC}$ | 4.5 V dc to +5.5 V dc |
| Minimum high-level input voltage, $V_{IH}$ | 2.2 V dc to $V_{CC}$ +1 |
| Maximum low-level input voltage, $V_{IL}$ | -0.1 to 0.80 V dc |
| High-level program input voltage, $V_{IH(PR)}$ | 24 to 26 V |
| Case operating temperature range | -55°C to +125°C |

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturerss in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the reference cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this specification. The truth table for programmed devices shall be as specified on figure 3.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance charcteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions | Device type | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|
| High-level output voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $V_{IN}$ = 2.4 V, $I_{OH}$ = -400 µA | 01 | 2.4 | | V |
| Low-level output voltage | $V_{OL}$ | $V_{CC}$ = 5.5 V, $I_{OL}$ = 2.1 mA | 01 | | 0.45 | V |
| Output leakage current | $I_{OL}$ 2/ | $V_{CC}$ = 5.5 V, PD/PGM = 2.4 V, $V_{OUT}$ = 5.5 V | 01 | | 10 | µA |
| High-level input current | $I_{IH}$ | Address, PD/PGM, $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.8 V | 01 | | 10 | µA |
| Low-level input current | $I_{IL}$ | Address, PD/PGM, $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.8 V | 01 | | 10 | µA |
| Supply current (standby) | $I_{SB}$ 4/ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 2.4 V, PD/PGM = $V_{IH}$, Outputs = Open | 01 | | 30 | mA |
| Supply current | $I_{CC}$ 4/ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 2.4 V, PD/PGM = $V_{IL}$, Outputs = Open | 01 | | 160 | mA |
| Program current | $I_{PP1}$ 4/ | $V_{PP}$ = 5.5 V, $V_{IN}$ = 2.4 V, PD/PGM = $V_{IL}$ | 01 | | 12 | mA |
| Output short circuit current | $I_{OS}$ | $V_{CC}$ = 5.5 V, Out = $V_{OH}$ | 01 | | -30 | mA |
| Input capacitance | $C_i$ | $V_i$ = 0 V, f = 1 MHz | 01 | | 6 | pF |
| Output capacitance | $C_o$ | $V_o$ = 0 V, f = 1 MHz | 01 | | 12 | pF |
| PD/PGM to programmed outputs | $t_{a(PR)}$ | $V_{CC}$ = 4.5 V to 5.5 V, See figure 4 | 01 | | 450 | ns |
| Address inputs to outputs (access time) | $t_{a(A)}$ | $V_{CC}$ = 4.5 V to 5.5 V, See figure 4, PD/PGM = $V_{IL}$ | 01 | | 450 | ns |
| Address to output hold | $t_{PVX}$ | $V_{CC}$ = 4.5 V to 5.5 V, See figure 4 or PD/PGM = $V_{IL}$ | 01 | 0 | | ns |
| PD/PGM high to output float | $t_{PXZ}$ | $V_{CC}$ = 4.5 V to 5.5 V, see figure 4 | 01 | 0 | 100 | ns |
| Read cycle time | $t_{c(RD)}$ | $V_{CC}$ = 4.5 to 5.5 V, see figure 4, PD/PGM = $V_{IL}$ | 01 | 450 | | ns |

1/ DC and read mode.

2/ Connect all address inputs and the PD/PGM input to $V_{IH}$ and measure $I_{OL}$ with the output under test connected through a current meter to the voltage specified.

3/ See table III for exact pin test conditions.

4/ $V_{PP}$ may be directly connected to $V_{CC}$ except during programming. The supply current would then be a sum of $I_{CC}$ and $I_{PP}$.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (see table III) |
|---|---|
| | Class B devices |
| Interim electrical parameters (pre burn-in) (method 5004) | 1 |
| Final electrical test parameters (method 5004) | 1*,2,3,7*,9 |
| Group A test requirements (method 5005) | 1,2,3,4,7,8, 9,10,11 |
| Group B test requirements (method 5005) | N/A |
| Group C end point electrical parameters (method 5005) | 1,2,3,7,8 |
| Group D end point electrical parameters (method 5005) | 1,2,3,7,8 |
| Additional electrical subgroups for group C periodic inspections | None |

NOTES:

1. (*) Indicates PDA applies to subgroup 1 and 7 (see 4.2c).
2. Any or all subgroups may be combined when using high-speed testers.
3. Subgroup 7 and 8 shall consist of verifying the binary count pattern.
4. For all electrical tests, the device shall be programmed to the pattern specified.

3.5 Electrical test requirements. Electrical test requirements shall be as specified in table II. The subgroups of table III which constitute the minimum electrical test requirements for screening and quality conformance, by device class, are specified in table II.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

3.7 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.7.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.8.

3.7.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7 and table IV.

3.7.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 47 (see MIL-M-38510, appendix E).

3.9 Manufacturer eligibility. To be eligible to supply microcircuits to this specification a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line, not necessarily the line producing the device described herein.

3.10 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2. Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883). Test condition D or E, using the circuit shown on figure 5 or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) for class B devices shall be 10 percent based on failures from group A, subgroups 1 and 7, test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the precent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

d. A programmability test shall be performed when programming the devices using an LTPD of 10.

e. A bit retention test shall be performed prior to burn-in and shall consist of the following:

(1) Program all devices with the complement of the binary count pattern (see 3.7.2 and 4.2d).

(2) Verify pattern (see 3.7.3).

(3) Remove all device terminal connections (including supply voltages).

(4) Perform a high temperature storage for 48 hours at 150°C.

(5) Restore device terminal connections.

(6) Verify pattern (see 3.7.3).

(7) Erase the pattern and program, devices with a binary count pattern (see 3.7.2).

(8) Verify pattern (see 3.7.3).

(9) Burn-in (see 4.2a).

(10) Verify pattern (see 3.7.3) at 25°C and at 125°C.

f. After completion of all testing, the devices shall be erased and verified prior to delivery (except devices submitted for groups A, B, C, and D testing).

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for group A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data maybe used to satisfy the requirements for group C and D inspections. (See paragraph 6.7)

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroup 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group B, C, and D testing.)

d. Subgroup 4 ($C_C$ and $C_O$ measurements) shall be measured only after process or design changes which may effect capacitance.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

a. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group C and D testing).

b. A special subgroup shall be added using an LTPD of 15 for class B. This subgroup shall consist of a high voltage test of the input protection circuits, $V_{ZAP}$ (see 4.9).

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

b. Steady state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D or E using the circuit shown on figure 5, or equivalent.

(2) $T_A$ = 125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

(4) All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

c. A reprogrammability test shall be added to group c inspection prior to performing the steady state life test (see 4.4.3b). The devices to be submitted to the steady state life testing shall be subjected to the following tests and examinations:

(1) Each device in the sample shall be subjected to a minimum of 50 program and erase cycles. Each cycle shall consist of the following steps.

(a) Program all devices with a binary count pattern.

(b) Verify pattern (see 3.7.3).

(c) Erase (see 3.7.1).

(d) Verify pattern (see 3.7.3).

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

b. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Inspection of packaging. The sampling and inspection of the preservation, packing, and container marking shall be in accordance with the requirements of MIL-M-38510.

4.7 Programming procedure. The following procedures shall be followed when programming and verification testing is performed. The waveforms and timing relationships shown on figure 6 and the test conditions and limits specified in table IV shall be adhered to.

a. Initially, and after each erasure, all bits are in the "H" state (output high). Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure.

b. The circuit is set up for programming operation by PD/PGM input to $V_{IH}$ and Vpp set to 25 V ±1.0 V. The word address is selected in the same manner as in the read mode. Data to be programmed, 8-Bits in parallel, are presented to the data lines ($O_1$-$O_8$). Logic levels for address and data lines, and the supply voltages are the same as for the read mode. After address and data set up, one program pulse ($V_{IL}$) per address is applied to the program input (Pin 20). The programming time for a single bit is only 50 ms and for all bits is approximately 200 seconds.

c. A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with Vpp at 25 V. PD/PGM shall be at $V_{IL}$.

4.8 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e. UV intensity X exposure time) is 15 W-s/cm$^2$. An example of an ultraviolet source which can erase the device in 30 minutes is the model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch away from the lamp tubes. After erasure, all bits are in the high state.

DEVICE TYPE 01

CASE J

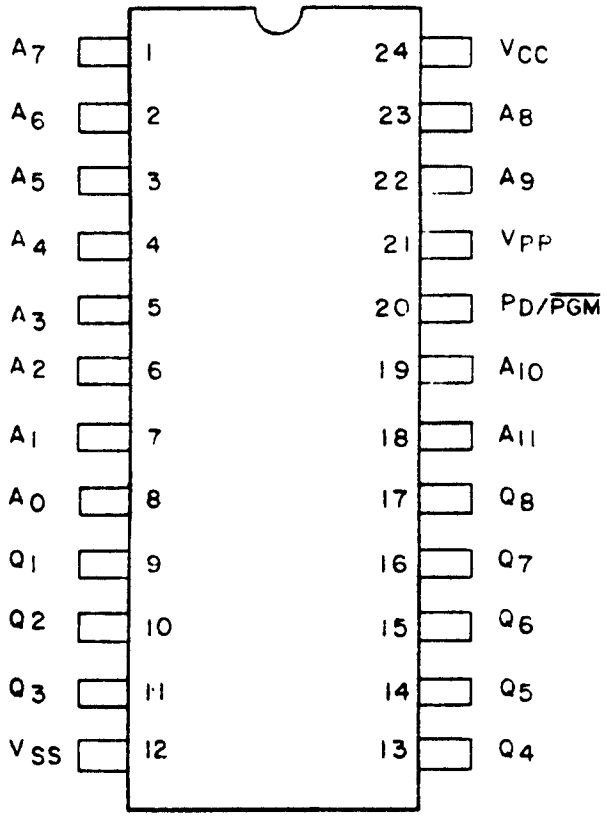



FIGURE 1. Terminal connections.

| Word Number | Inputs | | Outputs |
|---|---|---|---|
| | PD/$\overline{PGM}$ | $A_{11}$ ← → $A_0$ | $Q_8$ ← → $Q_1$ |
| X | GND | ← X → | H H H H H H H H |
| X | H | ← X → | ← Hi — Z → |

| Mode | | | | Outputs |
|---|---|---|---|---|
| | PD/$\overline{PGM}$ | $V_{PP}$ | $+V_{CC}$ | |
| Read | L | 5 V | 5 V | Data Out |
| Standby | H | 5 V | 5 V | High Z |
| Program | Pulsed L to H | 25 V | 5 V | Data In |
| Program Verify | L | 5 V | 5 V | Data Out |
| Program Inhibit | H | 25 V | 5 V | High Z |

1/ Positive Logic: H = High Logic Level
L = Low Logic Level
X = Irrelevant
HI-Z = High - Impedance State

2/ Outputs have internal active pull-ups.

FIGURE 2. Truth table.

DEVICE TYPE 01

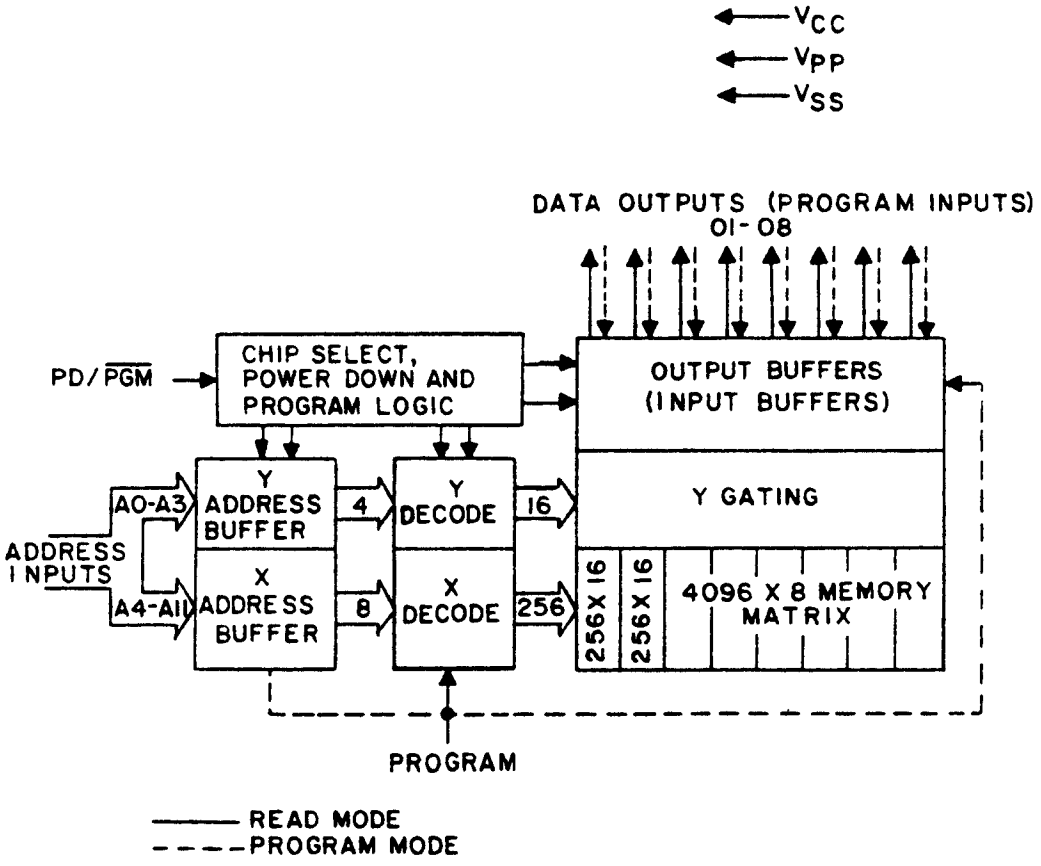
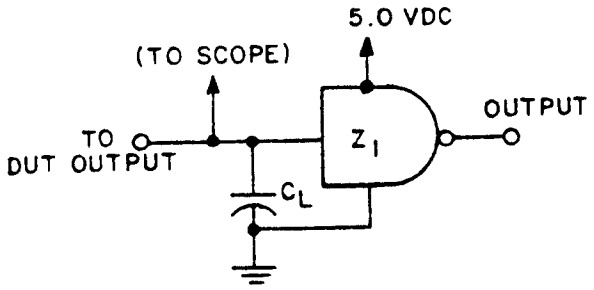
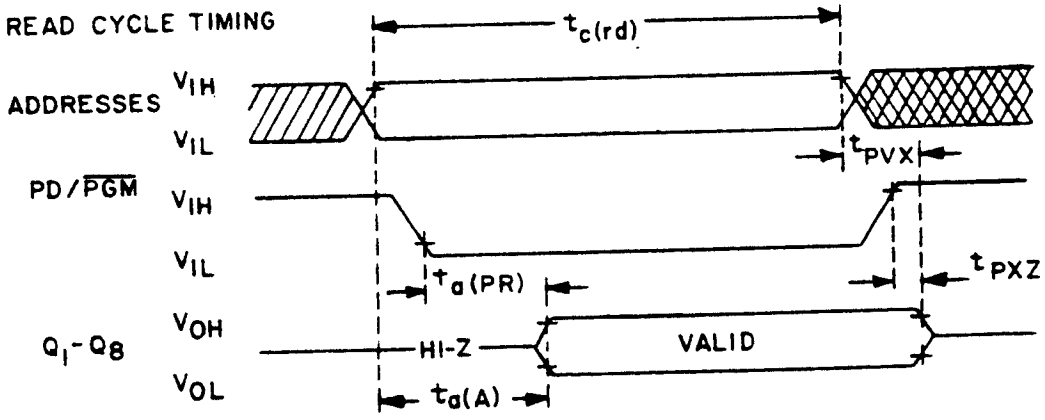


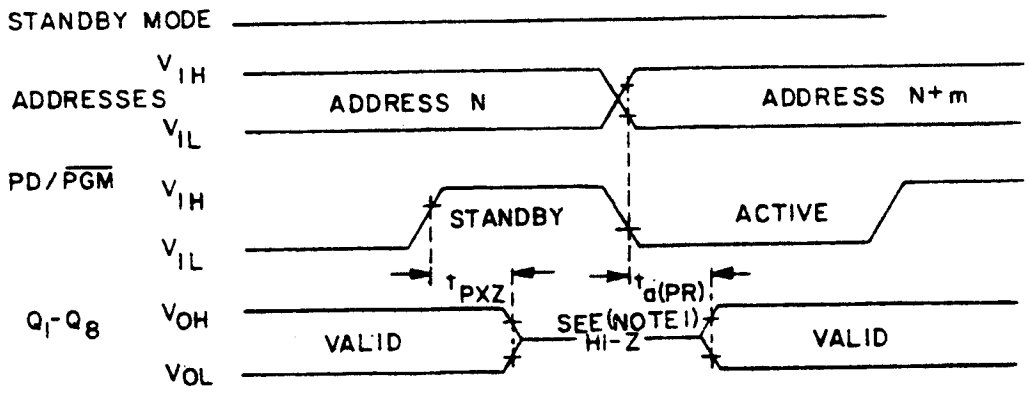

FIGURE 3. Functional block diagram.



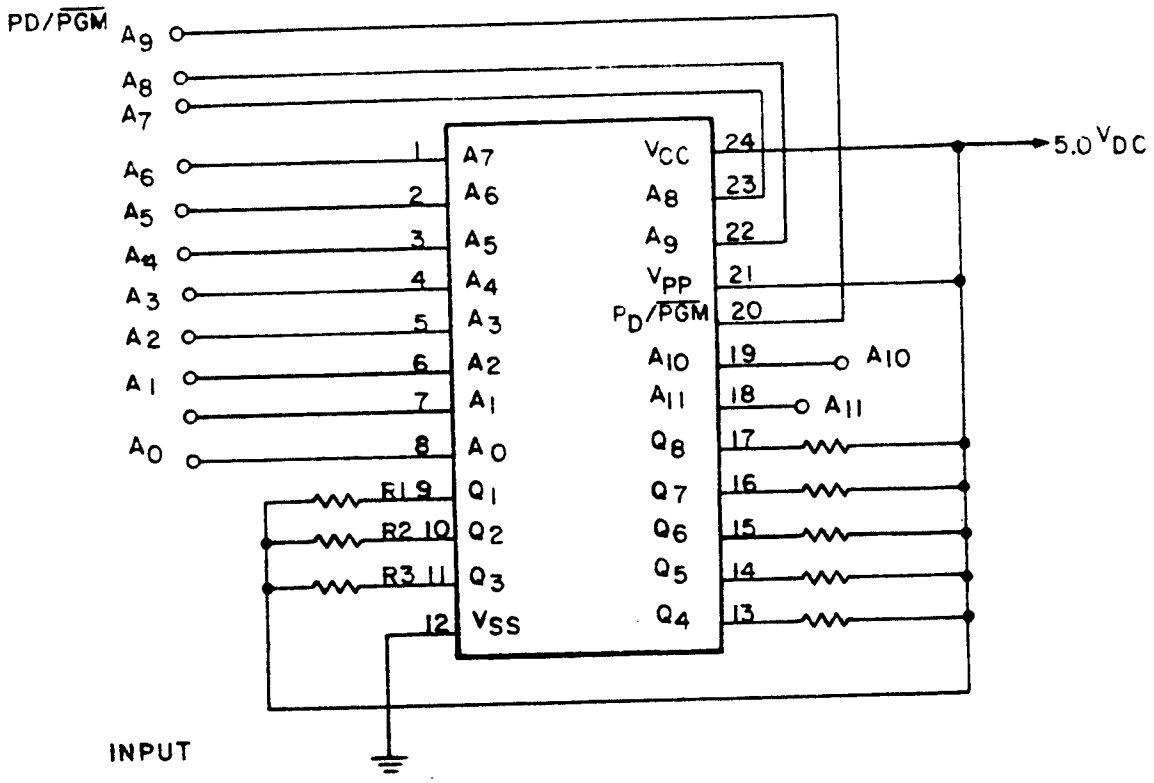

SEE NOTES AT END
OF FIGURE

FIGURE 4. Propagation delay time test circuit and waveform




NOTES:
1. $V_{CC}$ shall be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $C_L$ = 100 pF includes jig and probe capacitance. $Z_1$ = TTL gate or equivalent.
3. Input rise and fall times $\leq$ 20 nSec.
4. Input pulse levels 0.8 V to 2.2 V.
5. Timing measurement reference levels: Inputs 1.0 V and 2.0 V, Outputs 0.8 V and 2.0 V.
6. $t_a$ (PR) referenced to PD/$\overline{PGM}$ or the address, whichever occurs last.

FIGURE 4. Propagation delay time test circuit and waveforms - Continued.



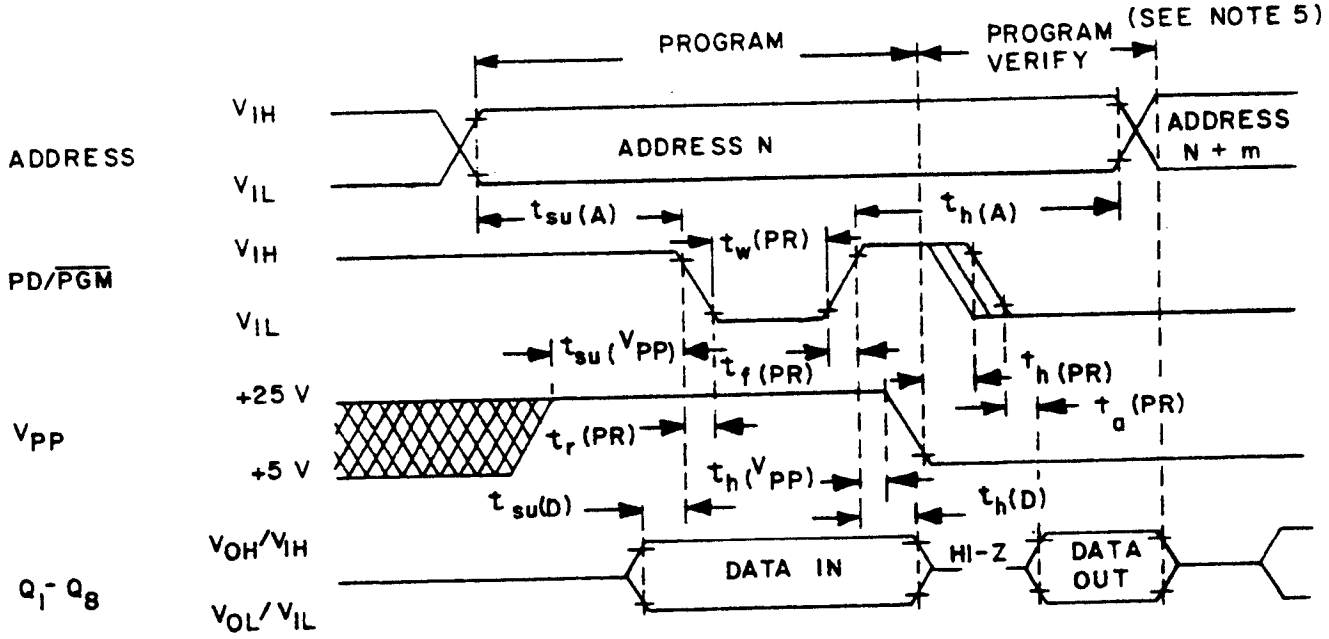

NOTES:
1. R1 thru R8 = 3.6 k Ohms ±5.0% when PD/$\overline{PGM}$ input is pulsed.
2. Input signal characteristics: Amplitude: $V_{IH} \geq 2.4$ V, $V_{IL} \leq 0.4$V; Duty Cycle = 50%; $t_{THL} \leq 100$ nSec and the following PRR (±20%).

| Input | PRR |
|---|---|
| $A_0$ | 16 KHz $\leq f_0 \leq$ 100 KHz |
| $A_1$ | $f_0 \div 2$ |
| $A_2$ | $f_0 \div 4$ |
| $A_3$ | $f_0 \div 8$ |
| $A_4$ | $f_0 \div 16$ |
| $A_5$ | $f_0 \div 32$ |
| $A_6$ | $f_0 \div 64$ |

| Input | PRR |
|---|---|
| $A_7$ | $f_0 \div 128$ |
| $A_8$ | $f_0 \div 256$ |
| $A_9$ | $f_0 \div 512$ |
| $A_{10}$ | $f_0 \div 1024$ |
| $A_{11}$ | $f_0 \div 2048$ |
| PD/$\overline{PGM}$ | $f_0 \div 4096$ |

FIGURE 5. Burn-in and steady state life test circuit.

PROGRAM CYCLE TIMING




NOTES:
1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10% to 90%) are 20 nSec.
4. Input pulse levels are 0.8 V to 2.2 V.
5. Program verify equivalent to read mode.

FIGURE 6. Programming waveforms.

TABLE III. Group A inspection device 01.

| Subgroup | Symbol | MIL-STD-883 method | Test no. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | Measured terminal | Test limits Min | Test limits Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | $O_1$ | $O_2$ | $O_3$ | GND | $O_4$ | $O_5$ | $O_6$ | $O_7$ | $O_8$ | $A_{11}$ | $A_{10}$ | PR/PGM | $V_{PP}$ | $A_9$ | $A_8$ | $V_{CC}$ | | | | |
| 1 $T_C$ = 25°C | $V_{OH}$ | 3006 | 1 2 3 4 5 6 7 8 | 1/ | 1/ | 1/ | 1/ | 1/ | 1/ | 1/ | 1/ | -400 µA | -400 µA | -400 µA | GND | -400 µA | -400 µA | -400 µA | -400 µA | -400 µA | 1/ | 1/ | 10.8 V | 14.5 V | 1/ | 1/ | 14.5 V | $O_1$ $O_2$ $O_3$ $O_4$ $O_5$ $O_6$ $O_7$ $O_8$ | 2.4 | | V |
| | $V_{OL}$ | 3007 | 9 10 11 12 13 14 15 16 | | | | | | | | | 2.1 mA | 2.1 mA | 2.1 mA | | 2.1 mA | 2.1 mA | 2.1 mA | 2.1 mA | 2.1 mA | | | | 5.5 V | | | 5.5 V | $O_1$ $O_2$ $O_3$ $O_4$ $O_5$ $O_6$ $O_7$ $O_8$ | | 0.45 | |
| | $I_{OL}$ 2/ | | 17 18 19 20 21 22 23 24 | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 5.5 V | 5.5 V | 5.5 V | | 5.5 V | 5.5 V | 5.5 V | 5.5 V | 5.5 V | 2.4 V | 2.4 V | 2.4 V | | 2.4 V | 2.4 V | | $O_1$ $O_2$ $O_3$ $O_4$ $O_5$ $O_6$ $O_7$ $O_8$ | | 10 | µA |
| | $I_{IH}$ | 3010 | 25 26 27 28 29 30 31 32 33 34 35 36 | 5.5 V | 5.5 V | 5.5 V | 5.5 V | 5.5 V | 5.5 V | 5.5 V | 5.5 V | | | | | | | | | | 5.5 V | 5.5 V | 10.8 V | | 5.5 V | 5.5 V | | $A_7$ $A_6$ $A_5$ $A_4$ $A_3$ $A_2$ $A_1$ $A_0$ $A_{10}$ $A_9$ $A_8$ $A_{11}$ | | | |
| | $I_{IL}$ | | 37 38 39 40 41 42 43 44 45 46 47 48 | 10.8 V | 10.8 V | 10.8 V | 10.8 V | 10.8 V | 10.8 V | 10.8 V | 10.8 V | | | | | | | | | | 10.8 V | 10.8 V | 10.8 V | | 10.8 V | 10.8 V | | $A_7$ $A_6$ $A_5$ $A_4$ $A_3$ $A_2$ $A_1$ $A_0$ $A_{10}$ $A_9$ $A_8$ $A_{11}$ | | | |
| | $I_{SB}$ | 3005 | 49 | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 2.4 V | 2.4 V | 2.4 V | | 2.4 V | 2.4 V | | $V_{CC}$ | | 30 | mA |
| | $I_{CC}$ | 3005 | 50 | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 2.4 V | 2.4 V | 10.8 V | 6.10 V | 2.4 V | 2.4 V | | $V_{CC}$ | | 180 | mA |
| | $I_{PP1}$ | 3005 | 51 | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 2.4 V | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 4/ | 2.4 V | 1/ | 10.8 V | 6.10 V | 2.4 V | 2.4 V | | $V_{PP}$ | | 12 | mA |
| 2 | Same tests, terminal conditions, and limits as subgroup 1, except $T_C$ = +125°C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | Same tests, terminal conditions, and limits as subgroup 1, except $T_C$ = -55°C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 $T_C$ = 25°C | $C_I$ | | 52 | | | | | | | | | | | | | | | | | | | | | | | | | All inputs | | 6 | pF |
| | $C_O$ | | 53 | | | | | | | | | | | | | | | | | | | | | | | | | All ouputs | | 12 | pF |
| 7 $T_C$ = 25°C | Functional tests | 3014 | 54 | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | All 1/ outputs | ≥1.0 | ≤1.0 | V |
| 8 | Same tests, terminal conditions, and limits as subgroup 7, except $T_C$ = +125°C and -55°C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

TABLE III. Group A inspection device 01 - Continued

| Subgroup | Symbol | MIL-STD-883 method | Test no. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | Measured terminal | Test limits Min | Test limits Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | $O_1$ | $O_2$ | $O_3$ | GND | $O_4$ | $O_5$ | $O_6$ | $O_7$ | $O_8$ | $A_{11}$ | $A_{10}$ | PR/PGM | $V_{pp}$ | $A_9$ | $A_8$ | $V_{CC}$ | | | | |
| 9 $T_C$ = 25°C | $t_{a(A)}$ | Fig. 4 | 55 | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | GND | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 7/ | 7/ | 6/ | 6/ | 7/ | All 7/ outputs | | 450 | ns |
| | $t_{a(PP)}$ | | 56 | | | | | | | | | | | | | | | | | | | | | | | | | | | 450 | |
| | $t_{PVX}$ | | 57 | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | | |
| | $t_{PXZ}$ | | 58 | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 100 | |
| | $t_{c(RD)}$ | | 59 | | | | | | | | | | | | | | | | | | | | | | | | | | 450 | | |
| 10 | Same tests, terminal conditions, and limits as subgroup 9, except $T_C$ = +125°C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | Same tests, terminal conditions, and limits as subgroup 9, except $T_C$ = -55°C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

1/ Before performing electrical tests, a binary count pattern shall be programmed into the devices submitted for acceptance. $V_{IH}$ (2.4 V) or $V_{IL}$ = 0.8 V shall be applied to the applicable address pins to set the measured terminal in the proper state for measurement.

2/ Connect all address inputs and the PD/PGM input to $V_{IH}$ and measure $I_{OL}$ with the output under test connected to the voltages specified.

3/ Not used.

4/ Output pins ($O_1$ thru $O_8$) shall be open.

5/ Tests shall verify binary count pattern by monitoring $t_{a(A)}$. All bits shall be tested with the following conditions:

a. $V_{CC}$ = 5.5 V

b. $V_{CC}$ = 4.5 V

c. Inputs: H = 2.2 V, L = 0.8 V.

d. Outputs: Output voltage shall be either,

(1) H = 2.4 V minimum and L = 0.8 V maximum when using a high speed checker double comparator.

(2) H ≥1.0 V and L ≤1.0 V when using a high speed checker single comparator.

6/ Each output shall be connected to the load circuit shown on figure 4 and propagation delay times shall be measured as follows:

a. PD/PGM input to programmed outputs. Condition address inputs $A_0$ thru $A_{11}$ to set outputs under test to the "L" state. Pulse PD/PGM input and measure $t_{a(A)}$.

b. Address inputs to outputs. Pulse PD/PGM input. Measure $t_{a(A)}$ from each address input to each output. Output under test shall be alternately changed from its low level to its high level by addressing the appropriate word combinations.

7/ See table I herein for supply voltages and test limits.

8/ $I_{OS}$ not tested.

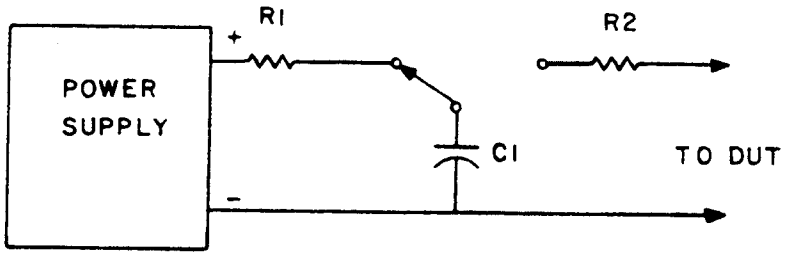
TABLE IV. Programming characteristics.
Recommended timing requirements for programming
$T_C$ = 25°C (see note 1)

| Parameter | | Min. | Typ+ | Max. | Unit |
|---|---|---|---|---|---|
| $t_{W(PR)}$ | Pulse width, program pulse | 45 | 50 | 55 | ns |
| $t_{r(PR)}$ | Rise time, program pulse | 5 | | | ns |
| $t_{f(PR)}$ | Fall time, program pulse | 5 | | | ns |
| $t_{su(A)}$ | Address setup time | 2 | | | µs |
| $t_{su(D)}$ | Data setup time | 2 | | | µs |
| $t_{su(VPP)}$ | Setup time from Vpp | 0 | | | ns |
| $t_{h(A)}$ | Address hold time | 2 | | | µs |
| $t_{h(D)}$ | Data hold time | 2 | | | µs |
| $t_{h(PR)}$ | Program pulse hold time | 0 | | | ns |
| $t_{h(VPP)}$ | Vpp hold time | 0 | | | ns |
| $I_{PP2}$ | Program pulse current | | | 30 | mA |

Typical values are at nominal voltages.

NOTES:
1. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and Vpp = 25 V +1 V during programming. All ac and dc measurements are made at 10% and 90% points with a 50% pattern.

2. Common test conditions apply for $t_{PXZ}$ except during programming. For $t_{a(A)}$ and $t_{PXZ}$, PD/PGM = $V_{IL}$.




$R_1$ = Appropriate current-limiting resistance
$R_2$ = 1.5 k Ohms ±5%
C1 = 100 pF ±20%
Power supply voltage = $V_{zap}$ = +150 VDC and -150 VDC.

FIGURE 7. High voltage ($V_{ZAP}$) test.

4.9 High voltage ($V_{ZAP}$) test of input protection circuit. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 150 volts from a 100-picofarad source in te following test sequence:

a. Measure $I_{IH}$ and $I_{IL}$ at one input terminal of the DUT at 25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of $I_{IH}$ and $I_{IL}$ shall be ±10 µA, maximum.

b. In the circuit below, charge the capacitor to -150 V. Then, using the same terminal of the device as selected above for leakage measurements, switch the capacitor to discharge into the device terminal. Then repeat the procedure with +150 V. (See figure 7).

c. Within 24 hours, repeat the $I_{IH}$ and $I_{IL}$ measurements on the same terminal as performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirement for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

$t_{c(rd)}$ - - - - - - - - - - - - - - - - Read cycle time

$t_{a(A)}$ - - - - - - - - - - - - - - - - Access time from address

$t_{a(PR)}$ - - - - - - - - - - - - - - - - Access time from PD/PGM

| | |
|---|---|
| $t_{pvx}$ - - - - - - - - - - - - - - - - | Output not valid from address change |
| $t_{pxz}$ - - - - - - - - - - - - - - - - | Output disable time from PD/PGM |
| PD/PGM - - - - - - - - - - - - - - - - - | Power down mode or/program pulse; output disable or output enable. |

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length and lead forming shall not affect the part number.

6.6 Handling. MOS devices shall be handled with certain precautions to avoid damage due to accumulation to static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS area.

f. Maintain relative humidity above 50 percent, if practical.

6.7 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the packaged represented. The vendor is required to retain generic data for a period of not less than 36 months from the date of shipment.

6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

6.10 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

| Military device type | Generic-industry type |
|---|---|
| 01 | 2532 |

Custodian:
Air Force - 17

Review activities:
Air Force - 11, 19, 85, 99
DLA - ES

Agent:
DLA - ES

Preparing activity:
Air Force - 17

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